IN THE CLAIMS

Please amend the claims as follows.

1-7. (Canceled).

8. (Previously Presented) An integrated circuit synchronous read channel for receiving digitized read signals representing digitized samples of a read signal of a magnetic storage device and recovering digital data represented thereby comprising:

a digital peak detector for detecting characteristics of the digitized read signals indicative of storage media transitions;

timing recovery circuitry responsive to the digitized read signals and the output of the digital peak detector to provide a timing control signal for controlling the timing of digitized samples of the read signal

a sequence detector responsive to the digitized read signals for receiving a stream of the digitized read signals and determining a corresponding sequence of binary digital signals likely to be represented thereby; and

an RLL (d,k) decoder for providing a run length limited decoded output by decoding the sequence of binary digital signals from the sequence detector, or to provide a run length limited decoded output by decoding a sequence of binary digital signals from the digital peak detector.

9. (Previously Presented) The integrated circuit synchronous read channel of claim 8 further comprising digital pulse shaping filter circuitry for modification of the digitized read signals prior to receipt thereof by at least one of (i) the sequence detector, (ii) digital peak detector and (iii) the timing recovery circuit.

10. (Previously Presented) An integrated circuit synchronous read channel for receiving digitized read signals representing digitized samples of a read signal of a magnetic storage device and recovering digital data represented thereby comprising:

a digital peak detector for detecting characteristics of the digitized read signals indicative of storage media transitions;

timing recovery circuitry responsive to the digitized read signals and the output of the digital peak detector to provide a timing control signal for controlling the timing of digitized samples of the read signal

a sequence detector responsive to the digitized read signals for receiving a stream of the digitized read signals and determining a corresponding sequence of binary digital signals likely to be represented thereby;

an RLL (d,k) decoder for providing a run length limited decoded output by decoding the sequence of binary digital signals from the sequence detector, or to provide a run length limited decoded output by decoding a sequence of binary digital signals from the digital peak detector;

digital pulse shaping filter circuitry for modification of the digitized read signals prior to receipt thereof by at least one of (i) the sequence detector, (ii) digital peak detector and (iii) the timing recovery circuit; and

delay means for delaying the coupling of the digitized read signals to the digital peak detector or the timing recovery circuit to match the delay of the coupling of the digitized read signals to the timing recovery circuitry or the digital peak detector, respectively, imposed by the digital pulse shaping filter.

11. (Previously Presented) The integrated circuit synchronous read channel of claim 9 wherein the digital pulse shaping filter circuitry includes variable filter parameters.

12. (Previously Presented) The integrated circuit synchronous read channel of claim 9 wherein the digital pulse shaping filter circuitry includes programmable filter parameters.

13. (Previously Presented) The integrated circuit synchronous read channel of claim 9 further comprising spectrum smoothing filter circuitry for filtering the digitized read signals prior to processing by the sequence detector.

14. (Previously Presented) An integrated circuit synchronous read channel for receiving digitized read signals representing digitized samples of a read

signal of a magnetic storage device and recovering digital data represented thereby comprising:

a digital peak detector for detecting characteristics of the digitized read signals indicative of storage media transitions;

timing recovery circuitry responsive to the digitized read signals and the output of the digital peak detector to provide a timing control signal for controlling the timing of digitized samples of the read signal

a sequence detector responsive to the digitized read signals for receiving a stream of the digitized read signals and determining a corresponding sequence of binary digital signals likely to be represented thereby; and

an RLL (d,k) decoder for providing a run length limited decoded output by decoding the sequence of binary digital signals from the sequence detector, or to provide a run length limited decoded output by decoding a sequence of binary digital signals from the digital peak detector,

wherein the sequence detector processes two digitized read signals at a time, the two digitized read signals representing digitized samples of a read signal of a magnetic storage device during two successive channel bit times.

15. (Previously Presented) The integrated circuit synchronous read channel of claim 8, wherein the sequence detector allows selection between center and side sampling of the digitized read signals.

16. (Previously Presented) The integrated circuit synchronous read channel of claim 8, wherein the sequence detector accommodates pulse asymmetry in the digitized read signals.

17. (Previously Presented) The integrated circuit synchronous read channel of claim 8, wherein the sequence detector is a partial response sequence detector.

18. (Previously Presented) The integrated circuit synchronous read channel of claim 8, wherein the timing recovery circuit operates in at least one of an acquisition mode and a tracking mode.

19. (Previously Presented) The integrated circuit synchronous read channel of claim 8, wherein the timing recovery circuit is programmable.

20. (Previously Presented) The integrated circuit synchronous read channel of claim 8, wherein the timing recovery circuit computes at least one of phase error and frequency error.

21. (Previously Presented) The integrated circuit synchronous read channel of claim 8, wherein the timing recovery circuit computes timing error at transition times.